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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/000,158	KHANNA ET AL.	
	Examiner	Art Unit	
	Hashem Farrokh	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *8/11/05*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-43,45-47,49-51,53,54 and 56-60* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-7,9-15,17-19,22-30,32-39,41-43,45-47,49-51,53-54,56-60-60* is/are rejected.

7)☒ Claim(s) *21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *11/01/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

This Office Action is in response to the Applicants' Remarks dated August 11, 2005. The instant application having application No. 10/000,158 has a total of 50 claims pending in the application; claims 1, 29, and 39 have been amended; claims 5, 8, 16, 20, 31, 40, 44, 48, 52, and 55 have been canceled; no new claims have been added.

INFORMATION CONCERNONG CLAIMS:

CLAIM OBJECTION

1. Claim 1 is objected to because of the following informalities:

The claim is marked "currently amended", *but there is no indication of any amendment in the body of the claim. The Examiner made a comparison between the current and previously provided claim and could not find any differences.*

Appropriate correction is required.

CLAIM REJECTION

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA

1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claim 14 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 6, 13 and 17 of copending Application No. 10/077,829. Although the conflicting claims are not identical, they are not patentably distinct from each other because of both claims the same invention as discussed below.

This is a provisional double patenting rejection since the conflicting claims have not in fact been patented.

2. ***Claim 14 of instant application (Application No. 10/000,158) are compared to claims 6, 13 and 17 of copending application (Application No. 10/077,829) in the following table:***

Application No. 10/077,829	Application No. 10/000,158
Claim 6: An apparatus, comprising:	**Claim 14:** An apparatus, comprising:

a content addressable memory (CAM) array to receive a comparand;	a content addressable memory (CAM) array to receive a comparand;
..., the translation circuitry having at least on first input, at least one second input, and at least one output,	a translation circuitry having at least on first input, at least one second input, and at least one output,
wherein the first input is configured to receive the input data	wherein the first input is configured to receive an input data having the plurality of bit groups,
wherein a first bit group has a first position in the input data relative to other bit groups,	wherein a first bit group has a first position in the input data relative to other bit groups,
wherein the second input is configured to receive the translation information indicative of translation of the first bit group from the first position to a different position in a comparand;	wherein the second input is configured to receive the translation information indicative of translation of the first bit group from the first position to a different position in a comparand;
the output coupled to the CAM array to	the output coupled to the CAM array to

This is not in the claims

transmit the comparand to the CAM array.	transmit the comparand to the CAM array,
Claim 13	
Wherein the translation circuitry comprises	wherein the translation circuitry comprises:
a storage element to store the translation information...	a storage element to store the translation information;
Claim 17	
a decode circuitry coupled to the plurality of selection circuitry to decode the portion of translation information and to establish a switch circuit connection between the first position and the position in comparand.	a decode circuitry coupled to the storage element to decode the translation information and to establish a connection in the switch circuit between the first position and position in comparand. a switch circuit;

There are some variation in the language of claims, however the both application teach same invention. For example the instant applicant (10/000,158) recite: " having the plurality of bit groups*". The limitation is inherent in the copending application* (10/077,829) where it recites: "wherein a first bit group has a first position in the input

data relative to other bit groups". *It is obvious that both claims have a plurality of bit groups. The claim 17 of Application (10/077,829) teaches the decode and switch circuitry recited in the claim 14 of the instant application for providing connection between the first position and the position in the comparand.*

Claim Rejections – 35 USC § 112

Claim 41 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Claim 41 is dependent from claim 40 that is a cancelled claim. In the following rejection of claim 41, the examiner has assumed that claim 41 is now depend from claim 39. The claim 41 must be amended to correct this error.

Claim Rejections - 35 USC § 102

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-4, 6-7, 9-14, 19, 22-25, 27-30, 33, 37-39, 41, 43, 45-47, 49—51, and 53-54 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent Publication No. 2004/0032775 A1 to Srinivasan et al. (hereinafter Srinivasan).

4. In regard to claim 1, Srinivasan teaches: "a method of operating a content addressable memory (CAM) device **(e.g., see paragraph 45, page 3)**, comprising:"

"comparing the comparand with data stored in a CAM array" **(e.g., see claim 3 in page 10).**

"receiving an input data **(e.g., see paragraph 13, page 2)** having a plurality of bit group," **(e.g., see paragraph 64, page 5; Fig. 6).** *For example field segment represents the bit group recited in the claim.*

"wherein a first bit group has a first position in the input data relative to the other bit group," **(e.g., see paragraph 64, page 5; Fig. 6).** *For example X1, shown in Fig. 6, has the first position with respect to the other segments.*

"wherein the input data has a second bit group having second position in the input data relative to the other bit group;" **(e.g., see paragraph 64, page 5; Fig. 6).** For example X2, shown in Fig. 6, has the second position with respect to the other segments.

"translating, in response to first translation information **(e.g., see paragraph 66, page 5)**, the first bit group from the first position to a different position in a comparand;" **(e.g., see paragraphs 56-57, page 4; paragraph 57, page 4; claim 6; Fig. 11).** *For example filter data (FDATA) represent the translation information.*

"translating the second bit group from the second position to second position of the comparand in response to second translation information;" **(e.g., see paragraphs 56-57, page 4; paragraph 57, page 4; claim 7; Fig. 11).**

"selecting the first translation information in a first cycle and the second translation information in a second cycle;" **(e.g., see paragraph 58, page 4).** *For example the reference teaches that the filtering can be performed concurrently or in sequence (e.g. first and second clock cycle).*

5. In regard to claims 2 and 50, Srinivasan teaches: "The method of claim 1, further comprising decoding the first translation information" **(e.g., see paragraph 79, page 7; element 1304 in Fig. 12).**

6. In regard to claims 3 and 51, Srinivasan teaches: "programming the CAM device with the first translation information" **(e.g., see paragraph 52, page 4).** *For example storing the lookup table in the CAM device represents programming the CAM device.*

7. In regard to claim 4, Srinivasan teaches: "wherein translating comprises establishing switch connection between the first position of the input data and the position of comparand" **(e.g., see paragraph 79, page 7; Fig. 7 and element 1304 in Fig. 12).** *For example crossbar switch makes connection between input string and the position in the comparand.*

8. In regard to claims 6-7 and 53-54, Srinivasan teaches: "sequentially translating the first and second bit group into the comparand." **(e.g., see paragraph 58, page 4).** *For example Srinivasan teaches that filtering/translation can be performed sequentially or concurrently.*

9. In regard to claims 9 and 22 Srinivasan teaches: "receiving the input data of a first width on an input bus of a second width, the first with being larger than the second width." **(e.g., see paragraph 11, pages 1-2).**

10. In regard to claim 10 and 23, Srinivasan teaches: "wherein the comparand has a third width being no greater than the second width of the input bus." **(e.g., see paragraph 68, page 5).**

11. In regard to claim 11, Srinivasan teaches: "wherein the first translation information determines the position of the comparand register that the first bit group is translated to" **(e.g., see paragraph 57, page 4; claim 6, page 10).** *For example* Srinivasan teaches that any bit/segments can be translated from input string to different point in the comparand.

12. In regard to claim 12, Srinivasan teaches: "wherein the first translation information determines which bit group of the plurality of bit groups is to be the first bit group translated to different position in the comparand" **(e.g., see paragraph 57, page 4; claim 6, page 10).** *For example* Srinivasan teaches that any bit/segments can be translated from input string to different point in the comparand based on the filter data (FDATA).

13. In regard to claims 13 and 27-28 Srinivasan teaches: "a processor coupled to the first input of the translation circuitry to transmit the input data" **(e.g., see paragraph 50, page 3; elements 310 and 320 in Fig. 3).**

14. In regard to claim 14, Srinivasan teaches: "An apparatus, comprising: a content addressable memory (CAM) array to receive a comparand" **(e.g., see paragraph 55, page 4; elements 410-414 in Fig. 4A).**

"a translation circuitry **(e.g., see paragraph 77, page 6; Fig. 11)** having at least on first input **(e.g., see element INPUT STRING in Fig. 11)**, at least one second input **(e.g., see element FDATA in Fig. 11)**, and at least one output, **(e.g., see paragraph 77, page 6; elements OUTPUT STRING in Fig. 11).** *For example Filter circuits 1200, shown in Fig. 11 represents the translation circuits recited in the claim.*

"wherein the first input is configured to receive an input data having the plurality of bit groups, **(e.g., see paragraph 64, page 5; Fig. 6).** *For example field segment represents the bit group recited in the claim.*

"wherein a first bit group has a first position in the input data relative to other bit groups," **(e.g., see paragraph 64, page 5; Fig. 6).** *For example X1, shown in Fig. 6, has the first position with respect to the other segments.*

"wherein the second input is configured to receive the translation information indicative of translation of the first bit group from the first position to a different position in a comparand;" **(e.g., see paragraphs 56-57, page 4; paragraph 57, page 4; claim 6; Fig. 11).** *For example Filter DATA (FDATA) represent the translation information. Based on the information provided by FDATA filtering or translations of segments or bit-groups are performed (e.g. translating bit-group to different position).*

"the output coupled to the CAM array to transmit the comparand to the CAM array" **(e.g., see paragraph 81, page 7; Fig. 4A; element OUTPUT STRING in Fig. 14).** *For example the output of filter circuits (e.g. OUTPUT STRING) coupled to CAM block (e.g. see Fig. 4A) to transmit the comparand to the CAM block.*

"and wherein the translation information comprises:"

"a switch circuit;" **(e.g., see paragraph 77, page 6; element 43 in Fig. 11).**

"a storage element to store the translation information;" **(e.g., see paragraph 55, page 4; paragraph 74, page 6; element PGM in Fig. 4B; element 1010 in Fig. 9).**

"and a decode circuitry coupled to the storage element to decode the translation information and to establish a connection in the switch circuit between the first position

and position in comparand." **(e.g., see paragraph 79, pages 6-7; paragraph 79, page 7; element 1206 in Fig. 14).** *For example the address generator includes decoders which is couple to the storage elements within the cross-bar switch to establish connection between the first input segment (or any input segment) and a position in comparand based on the stored translation information.*

15. In regard to claims 19 and 36, Srinivasan teaches: "wherein the switch circuit comprises a cross-bar switch" **(e.g., see paragraph 73, page 6; Fig. 9).**

16. In regard to claim 24, Srinivasan teaches: "a plurality of storage element, each of the plurality of storage element to store a portion of translation information;" **(e.g., see paragraph 82, page 7; element 1504 in Fig. 14).** *For example write buffer (e.g. element 1504) contains a plurality of storage elements to store the filter/translation information*

"selection circuitry coupled to plurality of storage element to select from the plurality of storage elements;" **(e.g., see paragraph 66, page 5; Fig. 7).** *For example the crossbar switch coupled to write buffer is programmed* to select from the plurality of storage elements

"and a decode circuit coupled to the plurality of selection circuitry to decode the portion of the translation information and to establish a switch circuit connection between the first position and the position in the comparand." **(e.g., see paragraph 99, page 9; elements 2114 and 430 in Fig. 21).** *For example the decode circuit coupled to crossbar switch and counter* to establish a switch circuit connection between the position in the field-segment of the input string and the comparand.

17. *In regard to claim 25, Srinivasan teaches*: "wherein each of the plurality of storage elements to store a portion of translation information for one cycle of plurality of cycles," **(e.g., see paragraph 73, page 6 elements 1010 in Fig. 9; element 1508 in Fig. 14).** *For example, in addition to block buffer register (BFR), crossbar switch contains additional storage elements (e.g. storage elements 1010).*

"and the selection circuitry to select from among the plurality of storage elements based on a particular cycle of plurality of cycles" **(e.g., see paragraph 99, page 9; elements 430, 1504, 1508, 2112, and 2114 Fig. 21).** *For example the decoder 2114 decode the sequential address provide for each cycle of the counter 2112 to select a rows of cross-bar switch, based on the information stored in the buffer register (1508)*

18. In regard to claim 29, Srinivasan teaches: "An apparatus, comprising: a content addressable memory (CAM) array having a plurality of blocks each configured to receive a comparand; and" **(e.g., see paragraph 55, page 4; elements 410-414 in Fig. 4A).**

"a plurality of translation circuitry," **(e.g., see paragraph 53, page 4; elements 420-424 in Fig. 4A).** *For example the filter circuits represent translation circuits.*

"each of the plurality of translation circuitry coupled to corresponding one of the plurality of CAM blocks," **(e.g., see paragraph 53, page 4; elements 410-414 and 420-424 in Fig. 4A).** *For example Fig. 4A shows that the outputs of filter circuits connected (coupled to the CAM blocks.*

"each translation circuitry **(e.g., see paragraph 77, page 6; Fig. 11)** having at least one first input **(e.g., see element INPUT STRING in Fig. 11)**, at least one second input

(e.g., see element FDATA in Fig. 11), and at least one output," **(e.g., see paragraph 77, page 6; elements OUTPUT STRING in Fig. 11).** *For example Filter circuits 1200, shown in Fig. 11 represents the translation circuits recited in the claim.*

"wherein the first input configured to receive an input data having a plurality of bit groups," **(e.g., see paragraph 64, page 5; Fig. 6).** *For example field segment represents the bit group recited in the claim.*

"wherein the first bit group has a first position in the input data relative to the other bit groups," **(e.g., see paragraph 64, page 5; Fig. 6).** *For example X1, shown in Fig. 6, has the first position with respect to the other segments.*

"wherein the second input is configured to receive translation information indicative of translation of the first bit group from the first position to different position in the comparand received by a respective CAM block," **(e.g., see paragraphs 56-57, page 4; paragraph 57, page 4; claim 6; Fig. 11).** *For example Filter DATA (FDATA) represent the translation information. Based on the information provided by FDATA filtering or translations of segments or bit-groups are performed (e.g. translating bit-group to different position).*

"the output coupled to the CAM array to transmit the comparand to the CAM block," **(e.g., see paragraph 81, page 7; Fig. 4A; element OUTPUT STRING in Fig. 14).** *For example the output of filter circuits (e.g. OUTPUT STRING) coupled to CAM block (e.g. see Fig. 4A) to transmit the comparand to the CAM block.*

"wherein each of the plurality of translation circuitry is configured to translate the plurality of bit groups over multiple operation cycles" **(e.g., see paragraph 58, page 4).**

For example the reference teaches that the filtering can be performed concurrently or in sequence (e.g. multiple clock cycles).

19. In regard to claim 30 Srinivasan teaches: "wherein each of the plurality of translation circuitry are configured to translate the plurality of bit groups over multiple operation cycles." **(e.g., see paragraph 58, page 4).** *For example Srinivasan teaches that filtering/translation can be performed sequentially or concurrently.*

20. In regard to claims 33 and 47 Srinivasan teaches: "wherein each of the translation circuitry comprises a switch circuit" **(e.g., see paragraph 55, page 4; elements 430-434 in Fig. 4B).** *For example Fig. 4B shows that each filter circuit contains a crossbar switch circuit, which represent the switch circuit recited in the claims.*

21. In regard to claim 37, Srinivasan teaches: "a plurality of storage element to store the translation information; and" **(e.g., see paragraph 83, page 7; elements 1508 in Fig. 14).** *For example Block Buffer Register (BFR) contains the translation information.* "a decode circuitry coupled to the plurality of selection circuitry to decode the portion of the translation information and to establish a switch circuit connection between the first position and the position in the comparand" **(e.g., see paragraph 99, page 9; elements 2114 and 430 in Fig. 21).** *For example the decode circuit coupled to crossbar switch and counter* to establish a switch circuit connection between the position in the field-segment of the input string and the comparand.

22. In regard to claims 38 Srinivasan teaches: "wherein two or more of the translation circuitry configured to concurrently establish the switch circuit." **(e.g., see paragraph**

58, page 4). *For example Srinivasan teaches that filtering/translation can be performed sequentially or concurrently.*

23. In regard to claim 39 Srinivasan teaches: "A content addressable memory (CAM) device, comprising: a CAM array to receive a comparand;" **(e.g., see paragraph 55, page 4; elements 410-414 in Fig. 4A).**

"a switch circuit having an input and an output, **(e.g., see elements INPUT STRING, OUTPUT STRING, and 430 in Figure 11).** *For example crossbar switch (XBAR) has at least one input and one output.*

"the input configured to receive input data having a plurality of bit groups," **(e.g., see paragraph 78, pages 6-7; element INPUT STRING in Fig. 11).**

"wherein a first bit group has a first position in the input data relative to other bit groups;" **(e.g., see paragraph 64, page 5; Fig. 6).** *For example X1, shown in Fig. 6, has the first position with respect to the other segments.*

"the output coupled to CAM array to transmit the comparand to the CAM array; " **(e.g., see elements OUTPUT STRING in Figure 11).**

"a storage element to store a translation information indicative of a translation of the first bit group from the first position to different position in the comparand." **(e.g., see paragraph 55, page 4; paragraph 74, page 6; element PGM in Fig. 4B; element 1010 in Fig. 9).**

24. In regard to claim 41, Srinivasan teaches: "a plurality of additional storage elements, the storage element and each of the plurality of additional storage elements to store a portion of translation information for one cycle of plurality of cycles;" **(e.g., see**

paragraph 73, page 6 elements 1010 in Fig. 9; element 1508 in Fig. 14). For example, in addition to block buffer register (BFR), crossbar switch contains additional storage elements (e.g. storage elements 1010).

"and selection circuitry coupled to the storage element and the plurality of additional storage elements to select from among the storage element and the plurality of additional storage elements based on a particular cycle of plurality of cycles for transmission to decode circuitry" **(e.g., see paragraph 83, page 7 elements 430 and 1504 in Fig. 14).**

25. In regard to claim 43, Srinivasan teaches: "An apparatus comprising: a content addressable memory (CAM) array;" **(e.g., see paragraph 55, page 4; elements 410-414 in Fig. 4A).**

"and means for translating **(e.g., see paragraph 77, page 6; Fig. 11)**, in response to translation information **(e.g., see paragraph 56, page 4)**, a bit group from a position of an input data having a plurality of bit groups to a different position in a comparand," **(e.g., see paragraphs 56-57, page 4; paragraph 57, page 4; claim 6; Fig. 11).** *For example Filter DATA (FDATA) represent the translation information. Based on the information provided by FDATA filtering or translations of segments or bit-groups are performed (e.g. translating bit-group to different position).*

"wherein the means for translating comprises: means for storing the translation information;" **(e.g., see paragraph 55, page 4; paragraph 74, page 6; element PGM in Fig. 4B; element 1010 in Fig. 9).**

"and means for decoding the translation information." **(e.g., see paragraph 79, page 7; element 1304 in Fig. 12).**

26. In regard to claim 45, Srinivasan teaches: "wherein the translating comprises means for selecting the translation information from a plurality of translation information" **(e.g., see paragraph 78, page 6; element 430 and 1208 in Fig. 11).**

27. In regard to claim 46, Srinivasan teaches: "An article comprising a machine readable medium that stores data representing an integrated circuit," **(e.g., see paragraph 44, page 3)**

"comprising:"

"a content addressable memory (CAM) array to receive a comparand" **(e.g., see paragraph 55, page 4; elements 410-414 in Fig. 4A).**

"a translation circuitry **(e.g., see paragraph 77, page 6; Fig. 11)** having at least one first input **(e.g., see element INPUT STRING in Fig. 11)**, at least one second input **(e.g., see element FDATA in Fig. 11)**, and at least one output," **(e.g., see paragraph 77, page 6; elements OUTPUT STRING in Fig. 11).** *For example Filter circuits 1200, shown in Fig. 11 represents the translation circuits recited in the claim.*

"wherein the first input is configured to receive an input data having the plurality of bit groups," **(e.g., see paragraph 64, page 5; Fig. 6).** *For example field segment represents the bit group recited in the claim.*

"wherein a first bit group has a first position in the input data relative to other bit groups," **(e.g., see paragraph 64, page 5; Fig. 6).** *For example X1, shown in Fig. 6, has the first position with respect to the other segments.*

"wherein the second input is configured to receive the translation information indicative of translation of the first bit group from the first position to a different position in a comparand;" **(e.g., see paragraphs 56-57, page 4; paragraph 57, page 4; claim 6; Fig. 11).** *For example Filter DATA (FDATA) represent the translation information. Based on the information provided by FDATA filtering or translations of segments or bit-groups are performed (e.g. translating bit-group to different position).*

"the output coupled to the CAM array to transmit the comparand to the CAM array" **(e.g., see paragraph 81, page 7; Fig. 4A; element OUTPUT STRING in Fig. 14).** *For example the output of filter circuits (e.g. OUTPUT STRING) coupled to CAM block (e.g. see Fig. 4A) to transmit the comparand to the CAM block.*

"the translation information comprises: a storage element to store the translation information;" **(e.g., see paragraph 55, page 4; paragraph 74, page 6; element PGM in Fig. 4B; element 1010 in Fig. 9).**

"and a decode circuitry coupled to the storage element to decode the translation information and to establish a connection in the switch circuit between the first position and position in comparand." **(e.g., see paragraph 79, page 7; element 1304 in Fig. 12).**

28. In regard to claim 49, Srinivasan teaches: "A content addressable memory (CAM) device, comprising:" **(e.g., see paragraph 55, page 4; elements 410-414 in Fig. 4A).**

"means for receiving an input data having a plurality of bit group," **(e.g., see paragraph 64, page 5; Fig. 6).** *For example field segment represents the bit group recited in the claim.*

"wherein a first group has a first position in the input data relative to the other bit group," **(e.g., see paragraph 64, page 5; Fig. 6).** *For example X1, shown in Fig. 6, has the first position with respect to the other segments.*

"wherein the input data has a second bit group having second position in the input data relative to the other bit group;" **(e.g., see paragraph 64, page 5; Fig. 6).** *For example X2, shown in Fig. 6, has the second position with respect to the other segments.*

"means for translating **(e.g., see paragraph 77, page 6; Fig. 11)**, in response to first translation information, the first bit group from the first position to a different position in a comparand;" **(e.g., see paragraphs 56-57, page 4; paragraph 57, page 4; claim 6; Fig. 11).** *For example Filter DATA (FDATA) represent the translation information. Based on the information provided by FDATA filtering or translations of segments or bit-groups are performed (e.g. translating bit-group to different position).*

"means for comparing the comparand with data stored in a CAM array" **(e.g., see column 4 lines 15-20, column 17 lines 67-68)**

"means for translating the second bit group from the second position to second position of the comparand in response to second translation information;" **(e.g., see paragraphs 56-57, page 4; paragraph 57, page 4; claim 6; Fig. 11).** *For example Filter DATA (FDATA) represent the translation information. Based on the information provided by*

FDATA filtering or translations of segments or bit-groups are performed (e.g. translating bit-group to different position).

"and means for selecting the first translation information in a first cycle and the second translation information in a second cycle;" **(e.g., see paragraph 58, page 4).** *For example the reference teaches that the filtering can be performed concurrently or in sequence (e.g. first and second clock cycle).*

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 15, 26, 32, and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over to Srinivasan in view of U.S. Patent 5,467,349 to Huey et al. (hereinafter Huey).

29. In regard to claims 15, 26, 32, and 42 Srinivasan teaches all limitations recited on the previous claims that these claims depend on but does not expressly teach: "comparand register(s) coupled between the CAM block(s) and translation circuits to store the comparand."

Huey teaches: "comparand register(s) coupled between the CAM block(s) and translation circuits to store the comparand." **(e.g., see paragrap 9, line 16; elements COMPARAND REGISTER in Fig. 11a)** for storing the VPI/VCI address into comparand

register. The disclosures by Huey is analogous to disclosure of Srinivasan, both references use CAM(s) for look-up table. Therefore, it would have been obvious to the one having ordinary skill in the art at the time the invention was made to include the comparand register(s) taught by Huey to the CAM blocks of Srinivasan, since the comparand register would provide storage for VC/VP address from compare bus and enables the address stored in the comparand register to be compared with data stored in the CAM array to determine whether there is a match **(e.g., see paragrap 9, lines 17-20)**

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Srinivasan in view of Huey as applied to claim 15 above, and further in view of U.S. Patent 5,978,307 to Proebsting et al. (hereinafter Proebsting).

30. In regard to claim 17, Srinivasan in view Huey of teaches all limitations recites in claim 15 but does not expressly teach: "wherein the switch circuit comprises at least one multiplexer"

Proebsting teaches: "wherein the switch circuit comprises at least one multiplexer" **(e.g., see column9, line 50; elements MUX 0 – MUX 383 in Fig. 4A)** *for selectively routing the bi-directional I/O lines to bit lines in the memory array. Disclosure by Proebsting is analogous to the disclosures by Srinivasan and Huey, they are all related to the memory devices. Therefore, it would have been obvious to one having ordinary skill in the art at the time invention was made to include multiplexer taught by Proebsting to the combined teaching of Srinivasan and Huey, since the inclusion of*

multiplexer would provide the capability to route relatively the smaller number of I/O lines to the substantially greater number of bit lines (e.g. see column 9, lines 64-67 and column 10, line 1).

Claims 18, 34-35, and 56-58 are rejected under 35 U.S.C. 103(a) as being unpatentable over to Srinivasan in view of Proebsting.

31. In regard to claims 18 and 35, Srinivasan teaches all limitations recites in claims 16 and 33 but does not expressly teach: "wherein the switch circuit comprises at least one demultiplexer"

Proebsting teaches: "wherein the switch circuit comprises at least one demultiplexer" **(e.g., see column9, line 50; elements DEMUX 0 – DEMUX 383 in Fig. 4A)** *for selectively routing the bi-directional I/O lines to bit lines in the memory array. Disclosures by Srinivasan and Proebsting are analogous and both are used to solve the same type of problem (e.g. routing in the memory). Therefore, it would have been obvious to one having ordinary skill in the art at the time invention was made to modify the switch taught by Srinivasan to include the demultiplexer disclosed by Proebsting, since the inclusion of demultiplexer would provide capability to route relatively the smaller number of I/O lines to the substantially greater number of bit lines (e.g. see column 9, lines 64-67 and column 10, line 1).*

32. In regard to claim 34, Srinivasan teaches all limitations recites in claims 33 but does not expressly teach: "wherein the switch circuit of at least one of the translation circuitry comprises at least one multiplexer"

Proebsting teaches: "wherein the switch circuit of at least one of the translation circuitry comprises at least one multiplexer" **(e.g., see column9, line 50; elements MUX 0 – MUX 383 in Fig. 4A)** *for selectively routing the bi-directional I/O lines to bit lines in the memory array. Disclosures by Srinivasan and Proebsting are analogous and both are used to solve the same type of problem (e.g. routing in the memory). Therefore, it would have been obvious to one having ordinary skill in the art at the time invention was made to modify the switch taught by Srinivasan to include the multiplexer disclosed by Proebsting, since the inclusion of multiplexer would provide capability to route relatively the smaller number of I/O lines to the substantially greater number of bit lines (e.g. see column 9, lines 64-67 and column 10, line 1).*

33 In regard to claim 56, Srinivasan teaches: "An apparatus comprising: a content addressable memory (CAM) array to receive a comparand" **(e.g., see paragraph 55, page 4; elements 410-414 in Fig. 4A).**

"a translation circuitry **(e.g., see paragraph 77, page 6; Fig. 11)** having at least one first input **(e.g., see element INPUT STRING in Fig. 11)**, at least one second input **(e.g., see element FDATA in Fig. 11)**, and at least one output," **(e.g., see paragraph 77, page 6; elements OUTPUT STRING in Fig. 11).** *For example Filter circuits 1200, shown in Fig. 11 represents the translation circuits recited in the claim.*

"wherein the first input is configured to receive an input data having the plurality of bit groups," **(e.g., see paragraph 64, page 5; Fig. 6).** *For example field segment represents the bit group recited in the claim.*

"wherein a first bit group has a first position in the input data relative to other bit groups," **(e.g., see paragraph 64, page 5; Fig. 6).** *For example X1, shown in Fig. 6, has the first position with respect to the other segments.*

"wherein the second input is configured to receive the translation information indicative of translation of the first bit group from the first position to a different position in a comparand;" **(e.g., see paragraphs 56-57, page 4; paragraph 57, page 4; claim 6; Fig. 11).** *For example Filter DATA (FDATA) represent the translation information. Based on the information provided by FDATA filtering or translations of segments or bit-groups are performed (e.g. translating bit-group to different position).*

"the output coupled to the CAM array to transmit the comparand to the CAM array," **(e.g., see paragraph 81, page 7; Fig. 4A; element OUTPUT STRING in Fig. 14).** *For example the output of filter circuits (e.g. OUTPUT STRING) coupled to CAM block (e.g. see Fig. 4A) to transmit the comparand to the CAM block. However,* Srinivasan does not expressly teach: "wherein the translation circuitry comprises a switch having at least one demultiplexer"

Proebsting teaches: "wherein the translation circuitry comprises a switch having at least one demultiplexer" **(e.g., see column9, line 50; elements DEMUX 0 – DEMUX 383 in Fig. 4A)** for selectively routing the bi-directional I/O lines to bit lines in the memory array. Disclosures by Srinivasan and Proebsting are analogous and both are used to solve the same type of problem (e.g. routing in the memory). Therefore, it would have been obvious to one having ordinary skill in the art at the time invention was made to modify the switch taught by Srinivasan to include the demultiplexer disclosed by

Proebsting, since the inclusion of demultiplexer would provide capability to route relatively the smaller number of I/O lines to the substantially greater number of bit lines (e.g. see column 9, lines 64-67 and column 10, line 1).

34. In regard to claim 57, Srinivasan further teaches: "a plurality of storage element, each of the plurality of storage element to store a portion of translation information;" **(e.g., see paragraph 82, page 7; element 1504 in Fig. 14).** *For example write buffer (e.g. element 1504) contains a plurality of storage elements to store the filter/translation information*

"selection circuitry coupled to plurality of storage element to select from the plurality of storage elements;" **(e.g., see paragraph 66, page 5; Fig. 7).** *For example the crossbar switch coupled to write buffer is programmed* to select from the plurality of storage elements

"and a decode circuit coupled to the plurality of selection circuitry to decode the portion of the translation information and to establish a switch circuit connection between the first position and the position in the comparand." **(e.g., see paragraph 99, page 9; elements 2114 and 430 in Fig. 21).** *For example the decode circuit coupled to crossbar switch and counter* to establish a switch circuit connection between the position in the field-segment of the input string and the comparand.

35. In regard to claim 58, Srinivasan further teaches: "wherein each of the plurality of storage elements to store a portion of translation information for one cycle of plurality of cycles," **(e.g., see paragraph 73, page 6 elements 1010 in Fig. 9; element 1508 in**

Fig. 14). *For example, in addition to block buffer register (BFR), crossbar switch contains additional storage elements (e.g. storage elements 1010).*

"and the selection circuitry to select from among the plurality of storage elements based on a particular cycle of plurality of cycles" **(e.g., see paragraph 99, page 9; elements 430, 1504, 1508, 2112, and 2114 Fig. 21).** *For example the decoder 2114 decodes the sequential address provide for each cycle of the counter 2112 to select a rows of cross-bar based on the information stored in the buffer register (1508)*

Claim 59-60 is rejected under 35 U.S.C. 103(a) as being unpatentable over Srinivasan in view of Proebsting as applied to claim 58 above, and further in view of Huey.

36. In regard to claim 59, Srinivasan in view of Proebsting teach all limitations recited in claim 58 but does not expressly teach: "a comparand register coupled between the CAM array and translation circuitry to store the comparand."

Huey teaches: comparand register coupled between the CAM block(s) and translation circuits to store the comparand." **(e.g., see paragrap 9, line 16; elements COMPARAND REGISTER in Fig. 11a)** *for storing the VPI/VCI address into comparand register. The disclosure by Huey is analogous to disclosures by Srinivasan and Proebsting, they are all related to memory. Therefore, it would have been obvious to the one having ordinary skill in the art at the time the invention was made to include the comparand register(s) taught by Huey to the combined teaching of Srinivasan and Proebsting, since the comparand register would provide storage for VC/VP address*

from compare bus and enables the address stored in the comparand register to be compared with data stored in the CAM array to determine whether there is a match (e.g., see paragrap 9, line 16).

37. *In regard to claim 60, Srinivasan further teaches:* "a processor coupled to the first input of the translation circuitry to transmit the input data" **(e.g., see paragraph 50, page 3; elements 310 and 320 in Fig. 3).**

ALLOWABLE SUBJECT MATTER

1. Claim 21 objected to as being dependent upon a rejected based claims, but would be allowable if rewritten in and independent form including all of the limitations of the base claim and any intervening claims.

The primary reason for allowance of claim 21 in instant application is the combination with the inclusion in this claim that the ***input bus coupled to first input of the translation circuit and wherein the switch circuit comprises a plurality of multiplexers each coupled to the input bus.***

: IMPORTANT NOTE :

I f the applicant should choose to rewrite the independent claims to include the limitations recited in either one of the claims, the applicant is encouraged to ***amend the title of the invention*** *such that it is descriptive of the invention as claimed as required be sec.* ***606.01*** *of the* ***MPEP****. Furthermore, the* ***summary of invention*** *and the* ***abstract***

should be amended to bring them into harmony with the allowed claims as required by paragraph 2 of ***sec. 1302.01*** *of the* ***MPEP****.*

As allowable subject matter has been indicated, applicant's response must either comply with all formal requirements or specifically traverse each requirement not compiled with. See ***37 C.F.R. § 1.111(b)*** *and* ***§ 707.07(a) of the M.P.E.P.***

Response to Applicants' Remarks

The Applicant's Remarks has been carefully considered but is not persuasive. In regard to segment or bit group translation from an input position to a position in the comparand, Srinivasan clearly teaches this limitation as references made in rejection of the claim. For example paragraph 66 in page 5 of Srinivasan teaches: "crossbar switch 720 is programmed by program data (PDATA) to select and translate or compact predetermined bits from input string 405 to output bit positions of the compacted filtered comparand string." (Emphasis added). *In paragraph 64 in page 5, Srinivasan teaches:* "The filtering of input string 405 may be performed by one or more of filter circuits 420-424, with each of filter circuits 420-424 programmed to filter different field segments of input string 405 or one or more of the same field segments. The filtering of input string 405 may be performed on a bit basis. Alternatively, the filtering of input string 405 may be performed based on other sizes, for example, a byte size. Moreover, each of filter circuits 420-424 may be re-programmed to filter different field segments of input string 405 from a prior programmed state." *Therefore Srinivasan teaches the translation portion recited in the claim.*

The claim limitations related to clock cycle recite: "selecting the first translation information in a first cycle and the second translation information in a second cycle". *Paragraph 58 in page 4 of Srinivasan teaches:* "In an alternative embodiment, the filtering of common input string 405 to generate the filtered comparand strings or search keys may be accomplished sequentially. The lookups in the blocks may also be performed concurrently or sequentially." *For example sequentially means one after another in an arranged way. For example the first translation information is selected in first cycle and the second translation information in the second cycle in sequence (e.g., second after first). Thus, Srinivasan teaches the claim limitations.*

Regarding claim 14, the Applicant argues: "Regarding claim 14, applicant submit that Srinivasan does not disclose the following limitation: a decode circuitry coupled to the storage element to decode the translation information and to establish a connection in the switch circuit between the first position and the position in the comparand..." *For example in paragraph 78, pages 6-9 Srinivasan discloses that programming circuit includes program data generator and address generator. In the same paragraph, Srinivasan teaches*: "Address generator 1206 may include, for example one or more row and/or column decoders to select one or more rows or column of intersections in the cross-bar switch for programming". *Therefore, the decoder coupled to the cross-bar switch that includes storage element for storing programming information and filtering or translating an input segment or bit-group from a bit-position to comparand. The applicant's argument regarding the other claims are very similar and the same response by the examiner would apply.*

Conclusion

The prior art made of record and not relied upon are as follows:

1. U. S. Patent No. 6,289,414 B1 to Feldmeier et al is a "Partially Ordered CAMS used in Ternary Hierarchical A address Searching/Sorting," describes a method of fast searches while reducing the search table size.

2. U. S. Patent No. 6,424,659 B2 to Viswanadham et al describes technique for network router implemented in ASIC, RISC processor, and software.

3. U. S. Patent No. 6,243,281 B1 to Pereira describing a method of accessing of CAM cells.

4. U. S. Patent Publication No. 20020015348 to Kanata et al describes a system and method power reduction in the CAM during the compare operation.

5. U. S. Patent Publication No. 2003/0039135 A1 to Srinivasan et al describes a method of filtering the input string to generate comparand string for a CAM device.

Any inquiry concerning this communication should be directed to Hashem Farrokh whose telephone number is (571) 272-4193. The examiner can normally be reached Monday-Friday from ***8:00 AM to 5:00 PM.***

If attempt to reach the above noted Examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Donald A Sparks, can be reached on (571) 272-4201. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published application may be obtained from either private PAIR or Public PAIR. Status information for unpublished application is available through Private PAIR only. For more information

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HF

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